

Notice of References Cited	Application/Control No. 10/792,153	Applicant(s)/Patent Under Reexamination ECCLES, ROBERT E.	
	Examiner Phallaka Kik	Art Unit 2825	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,021,513	02-2000	Beebe et al.	714/726
*	B	US-7,085,976	08-2006	Shirazi et al.	714/725
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Chen et al., "Design Verification of FPGA Implementations", IEEE Design & Test of Computers, Vol. 16, No. 2, April-June 1999, pp. 66-73.
	V	Brand, "Verification of Large Synthesized Designs", 1993 IEEE/ACM International Conference on Computer-Aided Design, 7 November 1993, pp. 534-537.
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.